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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($v_{GS} = 0$)	30	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	30	V
V_{GS}	Gate- source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$ dual operation	2	W

1. Pulse width limited by safe operating area

Table 2. Schottky absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		30	V
$I_{F(RMS)}$	RMS forward current		20	A
$I_{F(AV)}$	Average forward current	$T_L = 125^\circ\text{C}$ $\delta = 0.5$	3	A
I_{FSM}	Surge non repetitive forward current	$t_p = 10 \text{ ms}$ Sinusoidal	75	A
I_{RRM}	Repetitive peak reverse current	$t_p = 2 \mu\text{s}$ $F = 1 \text{ kHz}$	1	A
I_{RSM}	Non repetitive peak reverse current	$t_p = 100 \mu\text{s}$	1	A
dv/dt	Critical rate of rise of reverse voltage		10000	V/ μs

Table 3. Thermal data

R_{thj-a}	Thermal resistance junction-ambient MOSFET ⁽¹⁾	62.5	$^\circ\text{C/W}$ $^\circ\text{C/W}$
T_J	Junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$

1. Mounted on FR-4 board (steady state)

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage	$V_{DS} = \text{Max rating}$			1	μA
	Drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $T_C = 125^{\circ}C$			10	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 2A$		0.044	0.055	Ω
		$V_{GS} = 5V, I_D = 2A$		0.051	0.065	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 2A$		5		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		330		pF
C_{oss}	Output capacitance			90		pF
C_{rss}	Reverse transfer capacitance			40		pF
Q_g	Total gate charge	$V_{DD} = 24V, I_D = 4A,$ $V_{GS} = 5V$		6.5	9	nC
Q_{gs}	Gate-source charge			3.6		nC
Q_{gd}	Gate-drain charge			2		nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time	$V_{DD} = 15V, I_D = 2A,$ $R_G = 4.7\Omega, V_{GS} = 5V$ (see Figure 12)		11		ns
	Rise time			100		ns
$t_{d(off)}$ t_f	Turn-off delay time	$V_{DD} = 15V, I_D = 2A,$ $R_G = 4.7\Omega, V_{GS} = 5V$ (see Figure 12)		25		ns
	Fall time			22		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4A, V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 4A, V_{DD} = 15V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ (see Figure 14)		35		ns
Q_{rr}	Reverse recovery charge			25		nC
I_{RRM}	Reverse recovery current			1.4		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

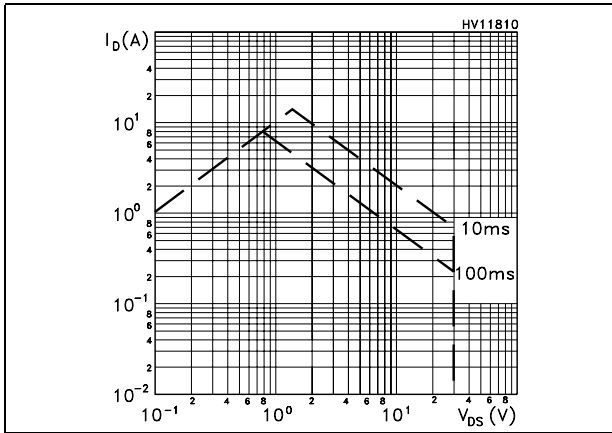


Figure 2. Thermal impedance

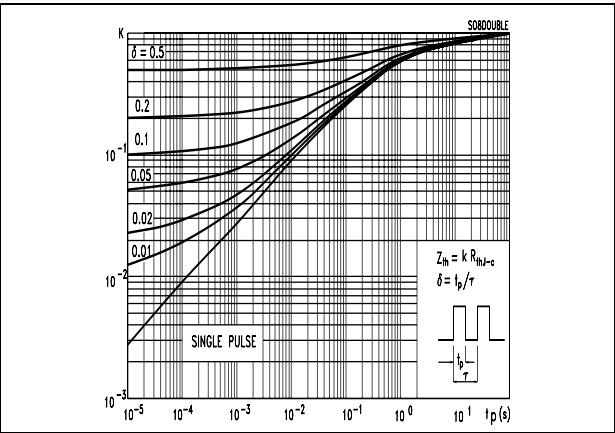


Figure 3. Output characteristics

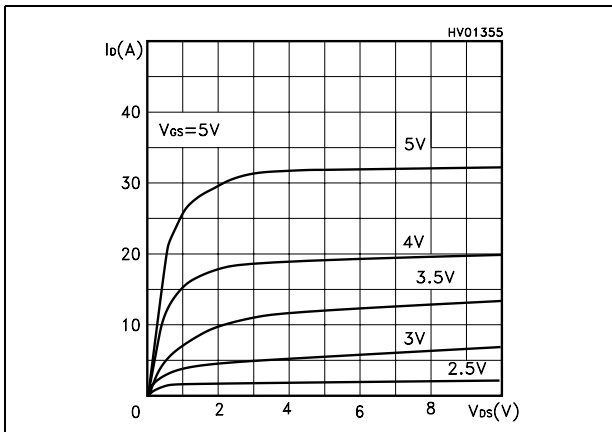


Figure 4. Transfer characteristics

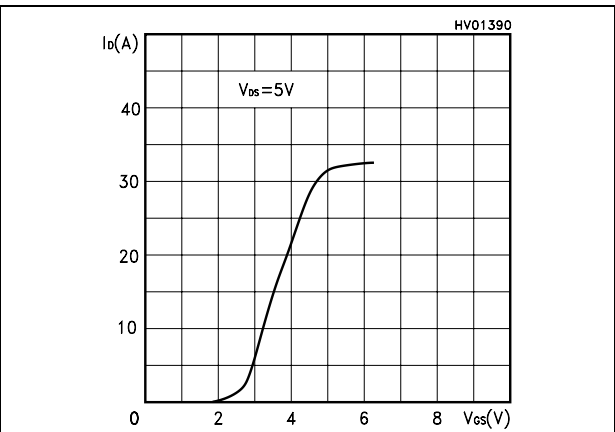


Figure 5. Transconductance

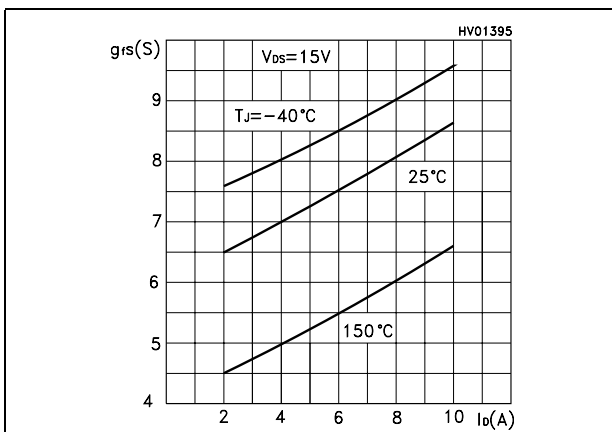


Figure 6. Static drain-source on resistance

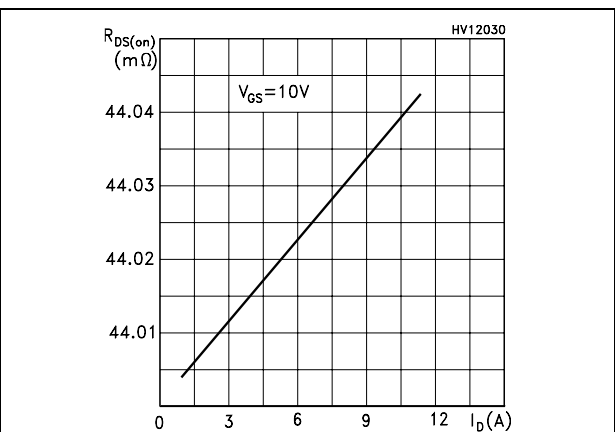


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

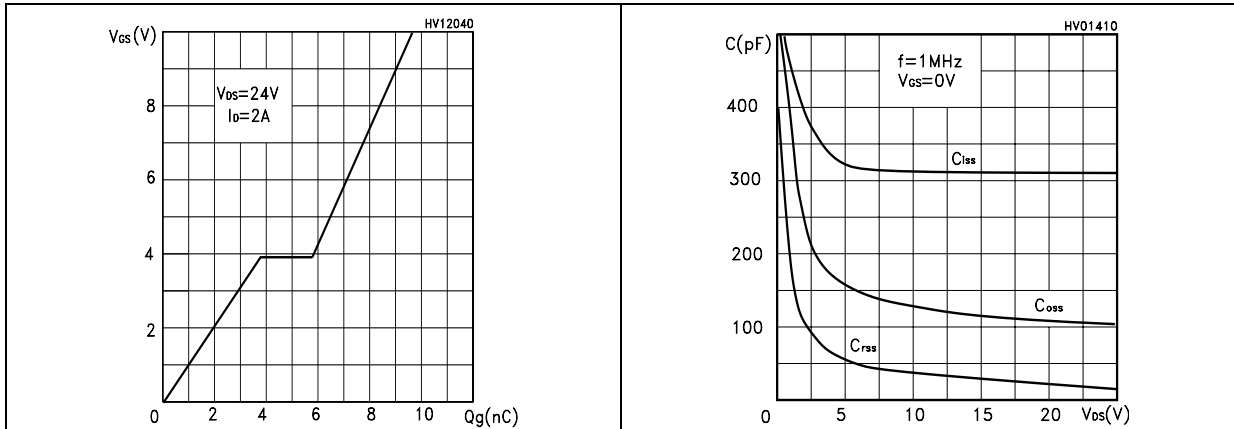


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

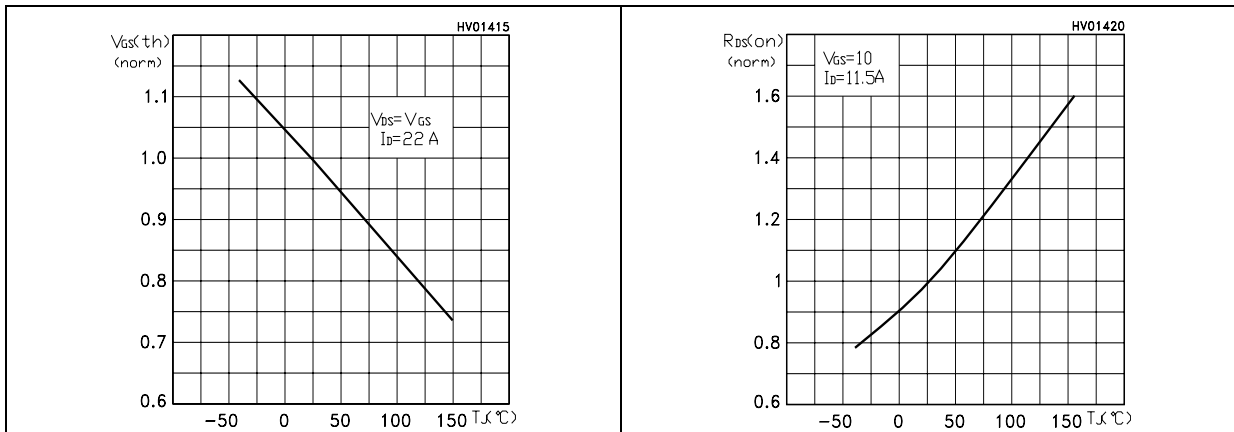
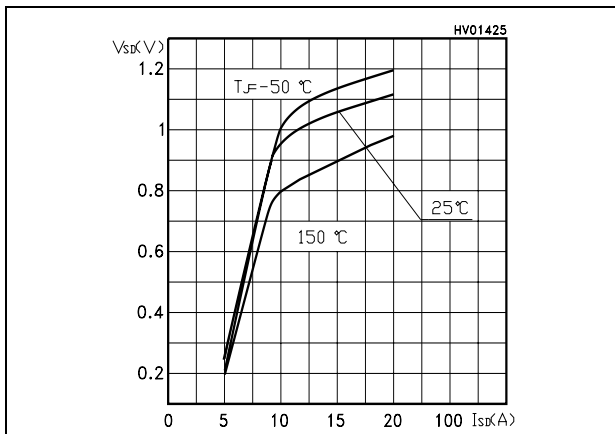


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit

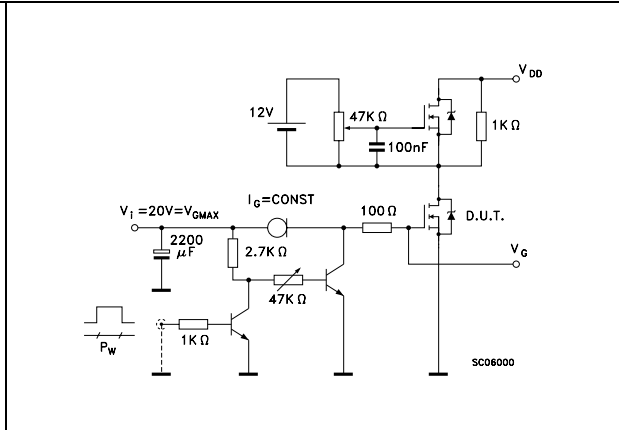


Figure 14. Test circuit for inductive load switching and diode recovery times

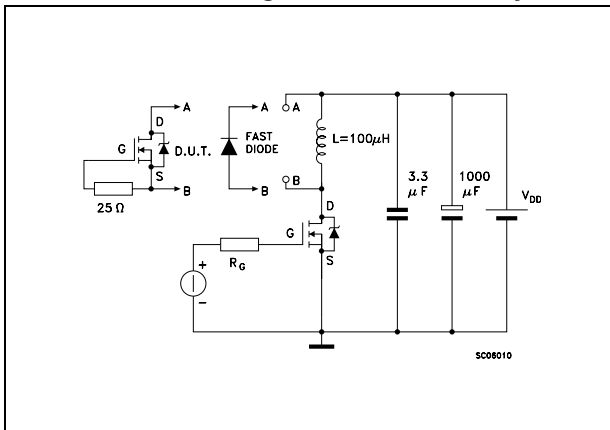


Figure 15. Unclamped Inductive load test circuit

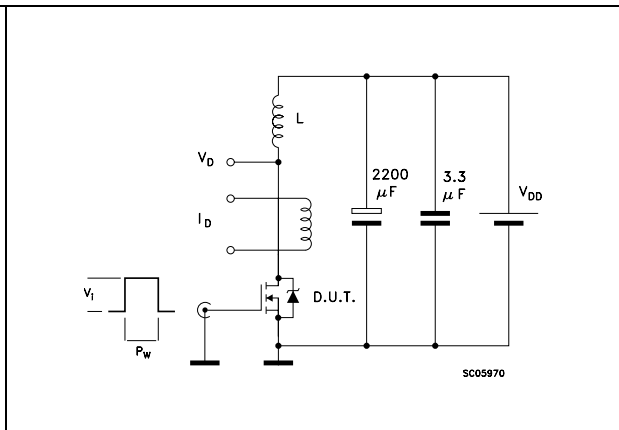


Figure 16. Unclamped inductive waveform

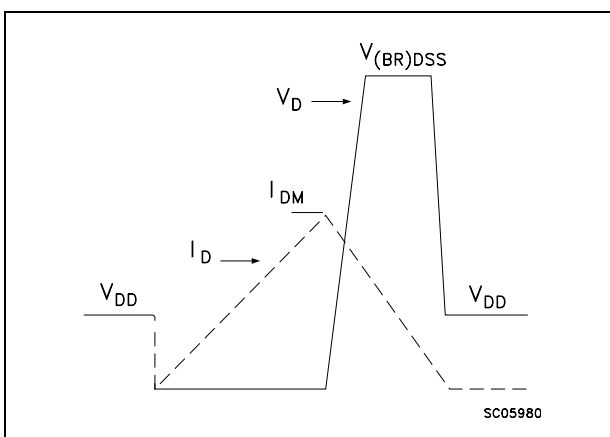
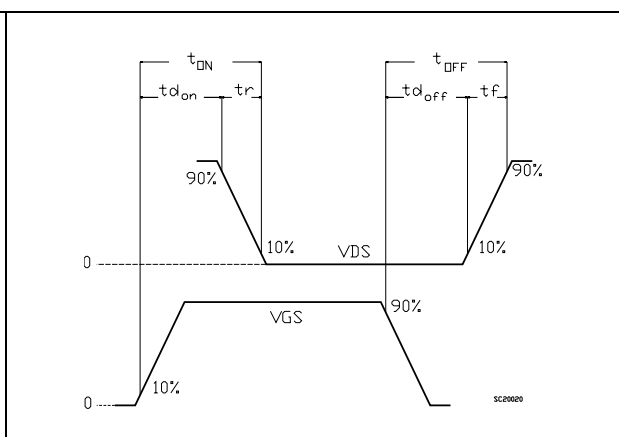


Figure 17. Switching time waveform

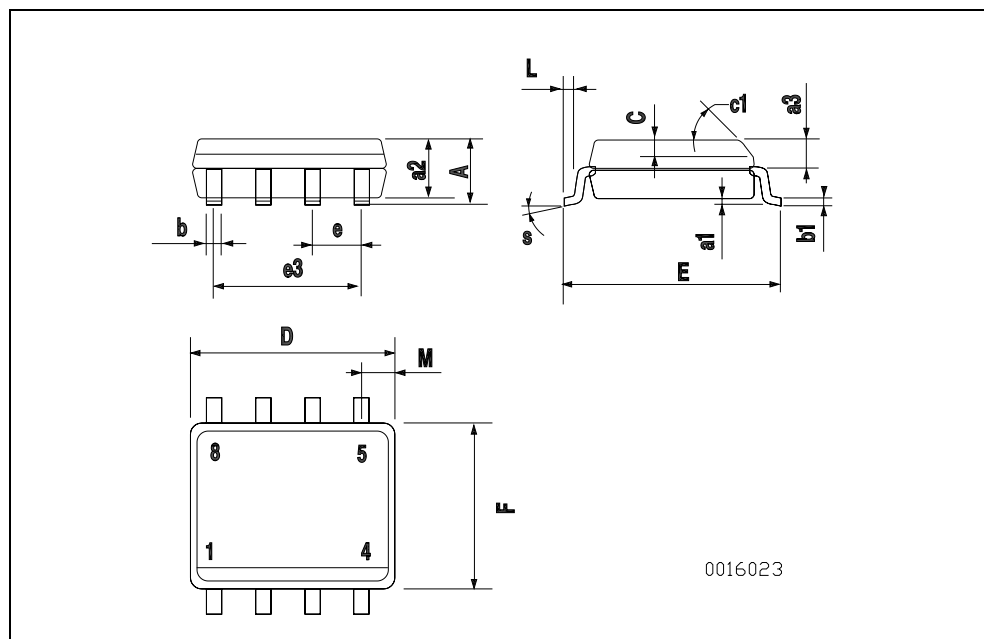


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	2	Complete version
10-Nov-2006	3	The document has been reformatted
26-Jan-2007	4	Typo mistakes on Table 1 .

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